(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 229 642 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
07.08.2002 Bulletin 2002/32

(51) Int Cl.[7]: **H03F 3/72**, H03F 1/02

(21) Application number: **01102249.8**

(22) Date of filing: **31.01.2001**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(71) Applicant: **Sony International (Europe) GmbH**
10785 Berlin (DE)

(72) Inventors:
- **Filinomov, Nicolai, Sony Inter. (Europe) GmbH**
Heisenbergbogen 1, 85609 Aschheim (DE)
- **Varlamov, Oleg,**
Sony International (Europe) GmbH
Heisenbergbogen 1, 85609 Aschheim (DE)

(74) Representative: **Körber, Martin, Dipl.-Phys. et al**
Mitscherlich & Partner
Patentanwälte
Sonnenstrasse 33
80331 München (DE)

(54) Power amplifier circuit for amplifying RF-Signals

(57) The present invention relates to a power amplifier circuit (1) for amplifying an input RF-signal comprising an amplification path (3) for amplifying an input RF-signal, a bypass path (5) for bypassing the amplification path (3) and a control terminal (6) for controlling the operation mode of the power amplifier circuit (1) between an amplifying mode and a bypassing mode, so that the input RF-signal is either amplified by the amplification path (3) in the amplifying mode or bypassed by the bypass path (5) in the bypassing mode.

The bypass path (5) is designed in a way, that it substantially does not affect the output RF-signal in the amplifying mode and that there is no need for a serial switch in the signal path of the bypass path (5).

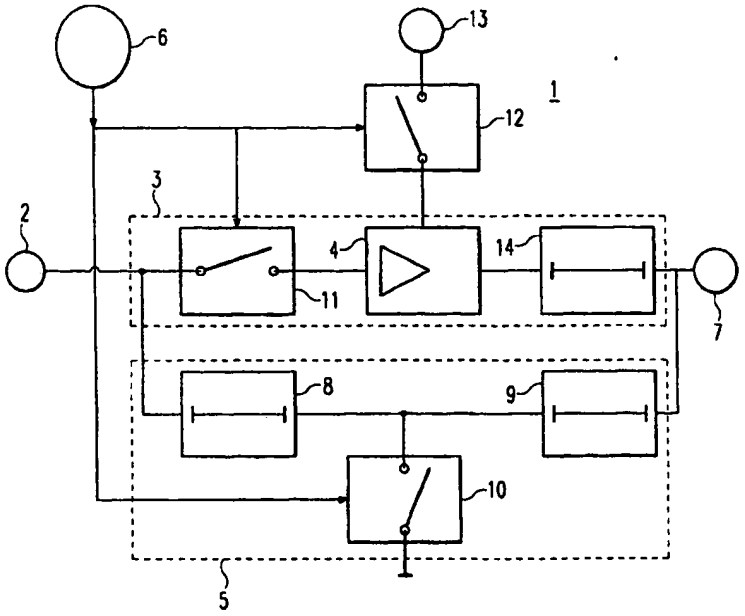

Fig. 1

EP 1 229 642 A1

Description

[0001] The present invention relates to a power amplifier circuit for amplifying an input RF-signal (radio frequency signal). It is particularly useful in the type of RF-signal power amplifiers used in wireless telephones.

[0002] Code Division Multiple Access (CDMA) modulation techniques are one of several techniques for facilitating communications in which a large number of system users are present. Although other techniques, such as time division multiple access (TDMA), frequency division multiple access (FDMA) are known, CDMA techniques have significant advantages over these other techniques. The CDMA techniques are used in many wireless telephone systems, such as IS-95, UMTS (with W-CDMA) and others.

[0003] In wireless telephone systems, a plurality of wireless telephones communicates with one or more base stations within "cells". In Code Division Multiple Access (CDMA) wireless telephone systems, in particular, wherein all portable users within a cell are sharing the same band of frequencies, but using different codes to modulate their respective signals, each wireless telephone transmitter signal becomes noise to all of the others. Keeping the overall noise level down tends to help all users. This is particularly true for UMTS, the W-CDMA standard. Wireless telephones are called upon to transmit at a wide range of power levels depending upon conditions existing at the time of transmission. A mobile W-CDMA phone is required to transmit at maximum power relatively seldom. For the greater part of the time it is better to transmit at relatively low power levels. When low power levels are required it is desirable that the current-consuming high-power stages be turned off and bypassed. Typically, W-CDMA wireless phones operate at a large number of discrete power levels; the levels are selected in response to changing transmission conditions.

[0004] The operating environment of a UMTS wireless telephone is typically urban or suburban. Both environments have common salient features: the probability of operating at high output power (such as more than 15 dBm), or at low output power (such as less than -15 dBm) is small. It is most probable that the power amplifier output power is in the neighbourhood of 0 - 10 dBm. Power amplifiers that are efficient at high output power (28 dBm) are usually not efficient at 5 dBm. The efficiency of class A amplifiers and class AB amplifiers tends to zero as the output power is reduced. High efficiency in the High Efficiency Power Amplifier sense refers to the average current drawn by the amplifier in a specified operating environment.

[0005] The cause of low efficiency in class A and class AB amplifiers at low output power is their idle or quiescent current. The level of quiescent current is chosen to satisfy the design requirements at maximum output power, but is typically still drawn from the supply when the power amplifier is not transmitting at maximum power. Since the power amplifier is seldom at maximum power the quiescent current is wasted most of the time.

[0006] A typical power amplifier consists of several serial stages. Each stage is usually larger, and more powerful than the previous one. Most of the quiescent current is drawn by latter high power stages, which are not required for the low output power levels at which the phone is often called upon to transmit. It follows that bypassing the high power stages when they are not required can make a significant saving in current.

[0007] Of course, the individual stages of a power amplifier add more than power, they add gain. Fortunately, the decrease in gain that accompanies bypassed stages is a bonus, as it decreases the dynamic range required by previous circuitry.

[0008] Since wireless telephones operate on battery power, it is also desirable that their transmitters operate as efficiently as possible to conserve power and extend battery life. Ideally for W-CDMA systems, such as those governed by the UMTS standard, power amplifier stages should be capable of efficient, linear operation over their required dynamic range. However, the prior art has not yet come close to the ideal and many wireless telephones are having poor power management now. During low power transmissions, power is wasted by cascaded amplifier stages that are not needed. Consequently, attempts have been made to bypass unused stages.

[0009] Such attempts have required the high power amplifiers output to pass through a switch. For example, see U.S. Pat. No. 5,661,434 issued August 26, 1997 to Brozovich et al. entitled "High Efficiency Multiple Power Level Amplifier Circuit". Brozovich et al. utilizes three single-pole single-throw switches to bypass stages of a multi-stage amplifier as shown in fig. 4. A bypass switch is always in series with the amplifier stage to be bypassed. However, it is difficult to utilize switches in series with high power amplifier stages. Generally, switches have a loss associated with them. Forcing the output of high power amplifier stages through a switch could cause an unacceptable loss. Furthermore, the types of switches that must be used for high power are both large and expensive, causing unacceptable design constraints.

[0010] In U.S. Pat. No. 6,069,526 issued May 30, 2000 to Ballantyne entitled "Partial or Complete Amplifier Bypass, the output bypass switch is eliminated. However, two switches with their losses remain in the signal path in the bypassing mode as shown in fig. 5.

[0011] It is therefore the object of the present invention, to provide a power amplifier circuit for amplifying RF-signals (radio frequency signals) comprising an amplification path for amplifying an input RF-signal and a bypass pass for bypassing an input RF-signal, which reduces the losses remain in the signal path in the bypassing mode in comparison to the prior art.

[0012] The above object is achieved by a power amplifier circuit for amplifying an input RF-signal, compris-

ing an input terminal featuring a first wave impedance Z_1 for inputting a RF-signal, an amplification path comprising an amplification means for amplifying the input RF-signal, a bypass path for bypassing the amplification path, a control terminal for controlling the operation mode of the power amplifier circuit between an amplifying mode and a bypassing mode, so that the input RF-signal is either amplified by the amplification path in the amplifying mode or bypassed by the bypass path in the bypassing mode, and an output terminal featuring a second wave impedance Z_2 for outputting the amplified or bypassed RF-signal.

[0013] The bypass path comprises a first matching circuit for adapting an input RF-signal to a third wave impedance Z_3, a second matching circuit for adapting the RF-signal adapted to the third wave impedance Z_3 to the second wave impedance Z_2 and for outputting the RF-signal adapted to the second wave impedance Z_2 to the output terminal, and a first switch controlled by the control terminal for changing the third impedance Z_3 so, that the bypass path substantially does not affect the output RF-signal in the amplifying mode, whereby the first switch is so disposed, that it is outside of the signal path of the bypass path in the bypassing mode.

[0014] In the amplifying mode (high power mode), an input radio frequency signal (RF-signal) is amplified by the amplification path. In this mode, the bypass path does not influence the operation of the amplification path.

[0015] In the bypassing mode (low power mode), an input RF-signal passes the power amplifier by to the output terminal through the bypass path. The amplification path in this mode does not affect the bypass path operation at all.

[0016] According to the present invention, there is no need for a serial switch within the bypass path. This has the advantage, that in the bypassing mode signal losses of the bypass path are reduced in comparison with prior art; the bypassed RF-signal passes the bypass path without considerable changes in signal power. The second switch, which is disposed in the amplification path, does substantially influence the RF-signal in the amplifying mode, since the RF-signal is gained by the amplification means 4 after the second switch.

[0017] For carrying out the present invention, the first switch switches the RF-signal adapted to the third wave impedance Z_3 to signal ground in the amplifying mode and disconnects the RF-signal adapted to the third wave impedance Z_3 from signal ground in the bypassing mode. Thereby, the third wave impedance Z_3 is much larger than the first and the second wave impedance Z_1 and Z_2.

[0018] In one embodiment of the present invention, the matching circuits respectively comprise at a time a transformer and a quarter wave transmission line for adapting the wave impedances.

[0019] In another embodiment of the present invention, the matching circuits comprise respectively a quarter wave transmission line with a wave impedance of $\mathrm{sqrt}(Z_1{*}Z_3)$ and $\mathrm{sqrt}(Z_2{*}Z_3)$ (sqrt= square root) for adapting the wave impedances.

[0020] Advantageously, the input wave impedance (first wave impedance Z_1) is equal to the output wave impedance (second wave impedance Z_2) of the power amplifier circuit; e.g. $Z_1=Z_2=50\Omega$. However it is also possible, that the power amplifier circuit according to the present invention operates as a impedance converter, for example featuring an input wave impedance (first wave impedance) of 50Ω and an output wave impedance (second wave impedance) of 75Ω.

[0021] The power amplifier circuit according to the present invention comprises a second switching means serial arranged in the amplification path controlled by the controlling means for connecting the amplification path to the input terminal in the amplifying mode and for disconnecting the amplification path from the input terminal in the bypassing mode.

[0022] Further, the power amplifier circuit comprises a third switching means controlled by the controlling means for connecting a power supply terminal to the amplification means in the amplifying mode and for disconnecting the power supply terminal from the amplification means in the bypassing mode. This has the advantage, that the power consumption of the amplification path tends to zero in the bypassing mode.

[0023] Further advantageously, the amplification path comprises a third matching circuit for adapting the output wave impedance of the amplification means to the second wave impedance Z_2 and for outputting the RF-signal to the output terminal.

[0024] The power amplify circuit according to the present invention is advantageously used in communication terminals for a wireless communication means like mobile phones in UMTS (Universal Mobile Telephone System).

[0025] In the following description, preferred embodiments of the present invention are explained in more detail in relation to the enclosed figures in which

figure 1 shows a schematic bloc diagram of the power amplifier circuit according to the present invention,

figure 2 shows a realization of the first and second matching circuit according to a first embodiment of the invention,

figure 3a shows a realization of the first and second matching circuit according to a second embodiment of the invention,

figure 3b shows a schematic representation of the equivalent circuit of the quarter wave transmission line of fig. 3a,

figure 4 shows a schematic representation of prior

art according to document US 5,661,434, and

figure 5 shows a schematic representation of prior art according to document US 6,069,526.

[0026] In Figure 1 the bloc diagram of an example of a power amplifier circuit 1 according to the present invention is shown. The power amplifier circuit 1 comprises basically the following units: a RF-input (input terminal 2), amplification means 4, control terminal 6, a RF-output (output terminal 7), first matching circuit 8, second matching circuit 9, first switch 10, second switch 11, third switch 12, power supply terminal 13 and third matching circuit 14.

[0027] The amplification path 3 comprises basically the second switch 11, amplification means 4 and third matching circuit 14. The bypass path 5 comprises basically the first and second matching circuit 8 and 9 and first switch 10.

[0028] A control means (not shown) is connected to the control terminal 6 for controlling the first, second and third switch 10, 11 and 12. For these purposes every switch comprises a control input at a time, which is connected at a time to the control terminal 6. The switches could for example realized by use of PIN-diodes as well as FET-transistors.

[0029] The input of the second switch 11 and the input of the first matching circuit 8 are connected to the input terminal 2. The output of the second switch 11 is connected to the input of the amplification means 4 and the output of the amplification means 4 is connected to the input of the third matching circuit 14, while the output of the third matching circuit 14 is connected to the output terminal 7.

[0030] The output of the first matching circuit 8 is connected to both the input of the second matching circuit 9 and the input of the first switch 10; the other input of the first switch 10 is shorted to ground. The output of the second matching circuit 9 is connected to the output terminal 7, the output of the third switch 12 is connected to the power input of the amplification means 4, and the input of the third switch 12 is connected to the power supply terminal 13. For supplying the power amplifier circuit 1 with power, a power supply (not shown) is connected to the power supply terminal 13.

[0031] It is also possible, to implement the third switch 12 into the amplification means 4. Since the third switch 12 switches DC-current power and no RF-signal, a low cost switch can be used.

[0032] The power amplifier circuit 1 according to the present invention operates in the following way:

[0033] In the amplifying mode (high power mode), an input radio-frequency signal is amplified by the amplification path 3, while the bypass path 5 in this mode does not influence the amplification path 3 operation. In the bypassing mode (low power mode), an input RF-signal passes to the power amplifier circuit 1 output through the bypass path 5 without considerable changes on signal power and the amplification path 3 in this mode does not affect the bypass path operation at all. Moreover, the consumption current of the amplification path 3 in the amplifying mode is equal to zero. As a result, when operating in the broad band of the required output power, a decrease in the average consumed current of the amplification means 4 is achieved.

[0034] To achieve a power consumption of the first, second and third switch 10, 11 and 12 and the amplification means 4 less than of that of the amplification means 4 in case of the amplification of an input signal to the level corresponding to the lower bound of the required output power in the amplifying mode, the first and second switch 10, 11 of the proposed power amplifier circuit 1 are opened in the bypassing mode. Therefore, with the technical realization of these switches using PIN-diodes as well as FET-transistors, their power consumption in the bypassing mode is equal to zero. Besides, the third switch 12 in the proposed power amplifier circuit 1 allows reducing the power consumption of the amplification means 4 to zero by means by switching off the power supply voltage from the amplification means 4 in the bypassing mode. Finally, the power consumption of the proposed power amplifier circuit 1 in the low power mode is equal to the power consumption of the third switch 12 in the turning off state of the amplifier means 4, and therefore it may be practically nullified.

[0035] The input and output impedance of the amplification path 3 in the bypassing mode should not considerably shunt the input and the output of the bypass path 5. This is achieved by the second switch 11 and the third matching circuit 14. The open second switch 11 prevents shunting the input of the bypass path 5 by the input impedance of the amplification path 3 in the bypassing mode. The third matching circuit 14 converts the output impedance of the amplification means 4 in turn-off state into the impedance that practically does not shunt the bypass path output. Such a matching circuit may be realized by a strip line segment with a characteristic wave impedance equal to the load impedance of the amplification means 4, and with a length that is adapted to convert the output impedance of the amplification means 4 in the turn-off state into an impedance that practically does not shunt the output of the bypass path 5. In this case, the third matching circuit 14 would not affect the amplification means 4 operation in the amplifying mode, since a strip line with the wave impedance equal to the load impedance has an input impedance equal to the load impedance.

[0036] In the bypassing mode, the gain should not significantly differ from 0dB, and in the amplifying mode, the input and the output impedance of the bypass path 5 should not considerably shunt the input and the output of the bypass path. This is achieved by the first and second matching circuit 8 and 9 on the one hand. They convert the low impedance of the closed first switch 10 into the high impedance that practically does not shunt the input and the output of the amplification path 3 in the

amplifying mode. On the other hand, these matching circuits provide the 0dB gain of the cascade connection of the first and second matching circuit 8 and 9, when the first switch 10 is open (i.e. the bypass path 5 in the bypassing mode).

[0037] When the input and the output of the amplification path 3 are practically not shunted by the bypass path 5 in the amplifying mode, the gain of the amplification path 3 does not significantly differ from the gain of the amplification means 4. Further, stability conditions of the power amplify circuit 1 according to the present invention are satisfied.

[0038] The operation of the bypass path 5 and the first and second matching circuit 8 and 9 is explained by the following examples in relation to figures 2 and 3a. In this examples, the first and second wave impedance Z_1 and Z_2 respectively are equal to 50Ω.

[0039] An idealized realization of a first bypass path design variant is shown in Fig. 2. This realization shows the structure of the first and second matching circuit 8 and 9 according to a first embodiment of the present invention.

[0040] The matching circuits 8 and 9 basically respectively comprises a transformer (transformer 1 and transformer 2) and a quarter wave transmission line (transmission line 1 and transmission line 2). In the bypassing mode, the first switch 10 is open and the bypass path represents a half-wave segment built of both quarter wave transmission lines with a wave impedance Z_3. The input of the first matching circuit 8 and the output of the second matching circuit 9 respectively are matched to the wave impedance of input terminal 2 and the output terminal 7 by means of appropriate transformers. This realization provides practically 0dB gain of the bypass path in the bypassing mode.

[0041] In the amplifying mode, the first switch 10 is closed and its impedance is equal to the closed switch impedance R_C. By means of the quarter-wave segments of the transmission lines transmission line 1 and transmission line 2, the third impedance Z_3 is converted into the third impedance Z_3' having a quantity of the order of $(Z_3)^2/R_C$, which is then converted by means of the transformers into a quantity of the order of $(Z_3*Z_1)/R_C$, which is the impedance with which the bypass path shunts the amplification path in the amplifying mode; in the bypassing mode (first switch open), Z_3' is equal to Z_3. For example, for Z_3=1000Ω, Z_1=50Ω and R_C=5Ω, the bypass path shunts the amplification path in 10000Ω-order quantity.

[0042] In other words, closing the first switch 10 leads to a high reflection of the transmitted RF-signal at the point of the connection of the first switch 10 with the bypass path, whereby the reflection factor depends on R_C; the lesser the quantity of R_C, the higher the reflection. Closing the first switch 10 further leads to a standing electromagnetic wave of the RF-signal in the quarter wave segment of transmission line 1, which prevents reflection of the RF-signal back to the input terminal and therewith into the amplification path.

[0043] The above described operation of the first matching circuit 8 for the input RF-signal of the power amplifier circuit according to the present invention is the same as of the second matching circuit 9 for the output RF-signal. Thus, the second matching circuit 9 prevents the RF-signal output by the amplification path from being reflected by the bypass path.

[0044] However, such a large value of Z_3 as in the example may be hardly implemented in practice with transformers. Thus, as an alternative way, the second variant of the bypass path design is proposed as shown in figure 3a. This variant differs from the first one in the way, that there is no impedance transformer-converter (transformer 1 and transformer 2), and the impedance conversion task is solved by the corresponding choice of the wave impedance of the quarter-wave transmission lines (transmission line 1 and transmission line 2). This wave impedance of the quarter wave transmission lines is chosen by the formula Z_{t1}=sqrt(Z_1*Z_3) and Z_{t1}=sqrt (Z_2*Z_3), where Z_3 is the calculated wave impedance value at the point of connection of the first switch 10 with the bypass path and Z_{t1} is the wave impedance of the quarter wave transmission line (transmission line 1 and transmission line 2). Under this conditions, the quarter wave transmission line 1 and quarter wave transmission line 2 may be realized using lumped elements as shown in Fig. 3b.

[0045] The operation of this second variant of bypass path implementation is absolutely identical with that of the first variant described above.

Claims

1. Power amplifier circuit (1) for amplifying an input RF-signal, comprising
   an input terminal (2) featuring a first wave impedance Z_1 for inputting a RF-signal,
   an amplification path (3) comprising an amplification means (4) for amplifying the input RF-signal,
   a bypass path (5) for bypassing the amplification path (3),
   a control terminal (6) for controlling the operation mode of the power amplifier circuit (1) between an amplifying mode and a bypassing mode, so that the input RF-signal is either amplified by the amplification path (3) in the amplifying mode or bypassed by the bypass path (5) in the bypassing mode, and
   an output terminal (7) featuring a second wave impedance Z_2 for outputting the amplified or bypassed RF-signal, whereby the bypass path comprises
   a first matching circuit (8) for adapting an input RF-signal to a third wave impedance Z_3,
   a second matching circuit (9) for adapting the RF-signal adapted to the third wave impedance Z_3 to the second wave impedance Z_2 and for outputting the RF-signal adapted to the second wave imped-

ance Z_2 to the output terminal (7), and
a first switch (10) controlled by the control terminal (6) for changing the third impedance Z_3 so, that the bypass path substantially does not affect the output RF-signal in the amplifying mode, whereby the first switch (10) is so disposed, that it is outside of the signal path of the bypass path in the bypassing mode.

2. Power amplifier circuit (1) according to claim 1, **characterized in**
that the first switch (10) switches the RF-signal adapted to the third wave impedance Z_3 to signal ground in the amplifying mode and for disconnecting the RF-signal adapted to the third wave impedance Z_3 from signal ground in the bypassing mode.

3. Power amplifier circuit (1) according to claim 1 or 2, **characterized in**
that the third wave impedance Z_3 is much larger than the first and the second wave impedance Z_1 and Z_2.

4. Power amplifier circuit (1) according to claim 1, 2 or 3, **characterized in**
that the matching circuits (8, 9) respectively comprise a transformer and a quarter wave transmission line for adapting the wave impedances.

5. Power amplifier circuit (1) according to claim 1, 2 or 3, **characterized in**
that the first matching circuit (8) comprises a quarter wave transmission line with a wave impedance of sqrt(Z_1*Z_3) and the second matching circuit (9) comprises a quarter wave transmission line with a wave impedance of sqrt(Z_2*Z_3) for adapting the wave impedances.

6. Power amplifier circuit (1) according to one of the claims 1 to 5, **characterized in**
that the first wave impedance Z_1 is equal to the second wave impedance Z_2.

7. Power amplifier circuit (1) according to one of the claims 1 to 6, **characterized in**
that the amplification path (3) comprises a second switching means (11) controlled by the controlling means (6) for connecting the amplification path (3) to the input terminal (2) in the amplifying mode and for disconnecting the amplification path (3) from the input terminal (2) in the bypassing mode.

8. Power amplifier circuit (1) according to one of the claims 1 to 7, **characterized by**
a third switching means (12) controlled by the controlling means (6) for switching a power supply terminal (13) to the amplification means (4) in the amplifying mode.

9. Power amplifier circuit (1) according to one of the claims 1 to 8, **characterized in**
that the amplification path (3) comprises a third matching circuit (14) for adapting the output wave impedance of the amplification means (4) to the third wave impedance Z_3 and for outputting the RF-signal to the output terminal (7).

10. Portable communication terminal for a wireless communication system, comprising
a power amplifier circuit (1) according to one of the claims 1 to 9.

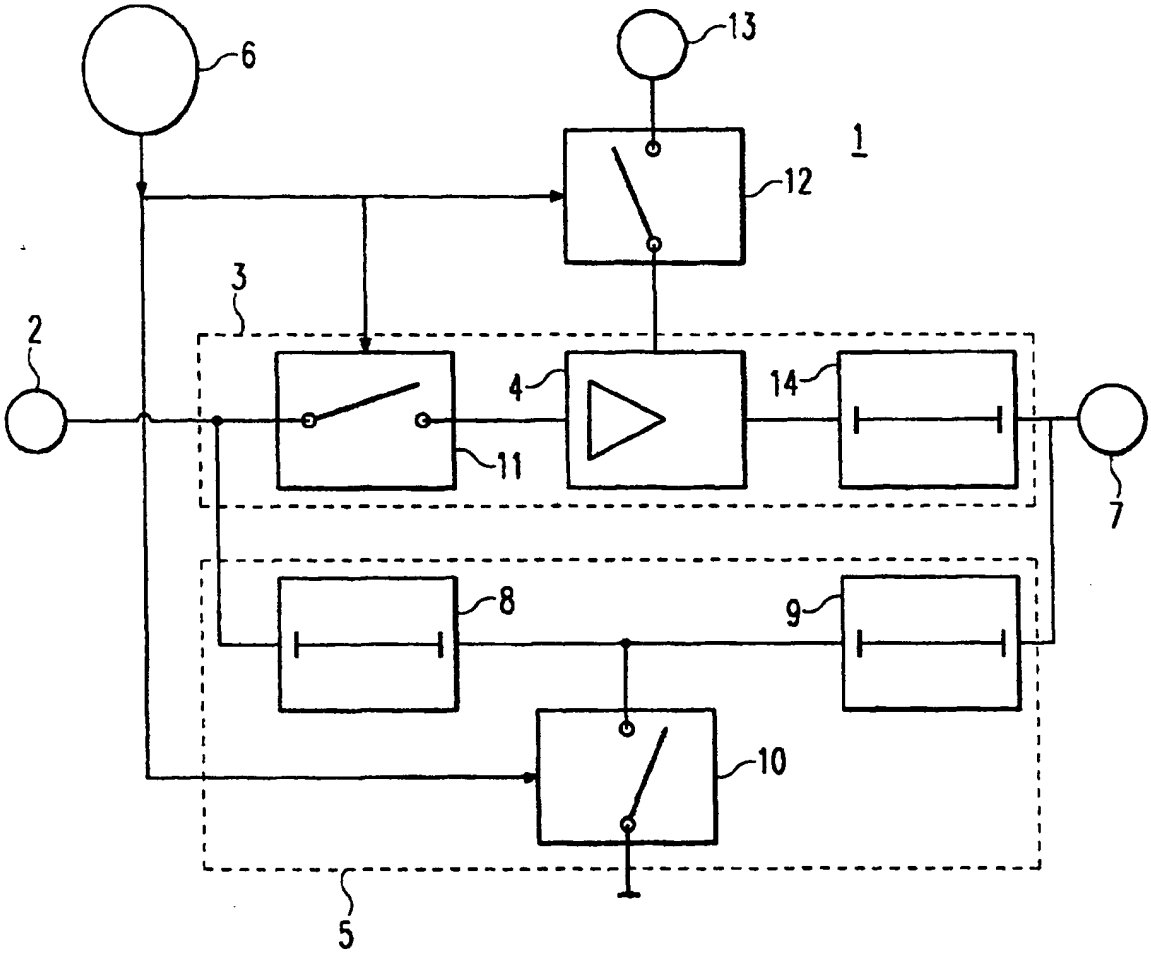

Fig. 1

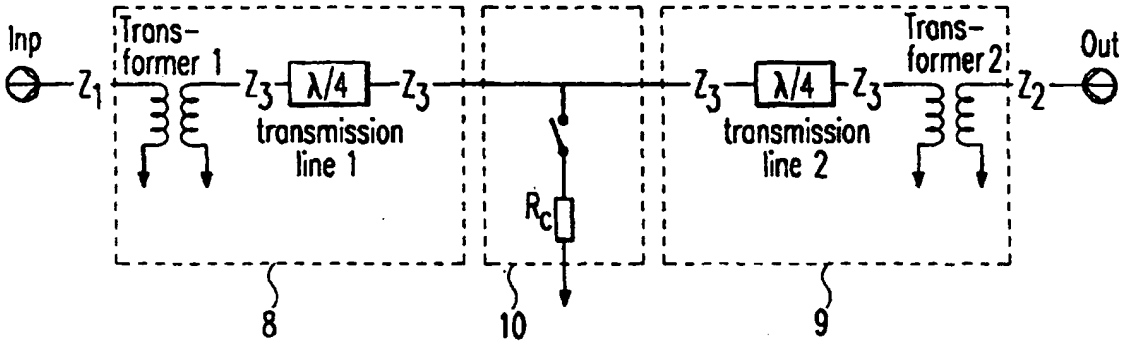

Fig. 2

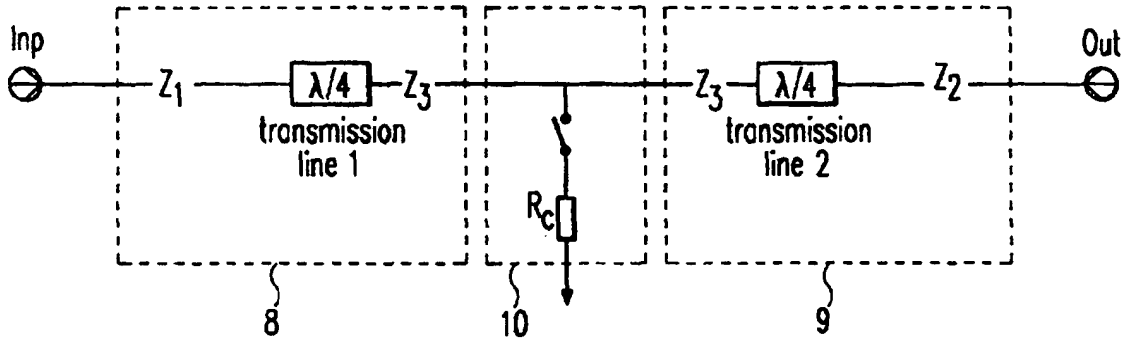

Fig. 3a

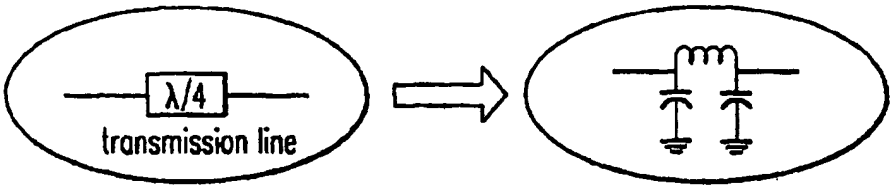

Fig. 3b

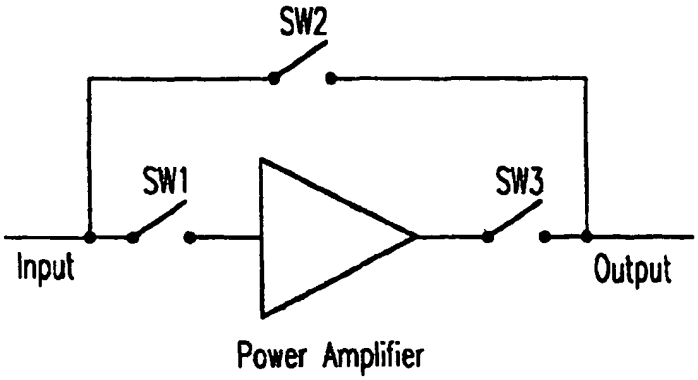
SW2
SW1
SW3
Input
Output
Power Amplifier

Fig. 4

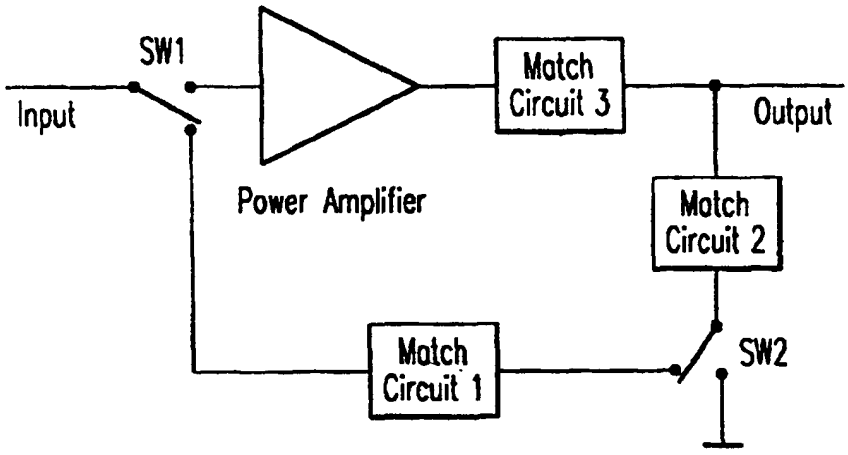
SW1
Input
Power Amplifier
Match Circuit 3
Output
Match Circuit 2
Match Circuit 1
SW2

Fig. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 10 2249

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	EP 1 032 120 A (MATSUSHITA ELECTRIC IND CO LTD) 30 August 2000 (2000-08-30) * page 10, line 7 - line 58; figure 8 * ---	1,2,4,5, 7-9	H03F3/72 H03F1/02
A	EP 0 837 559 A (MATSUSHITA ELECTRIC IND CO LTD) 22 April 1998 (1998-04-22) * page 11, line 32 - line 54; figure 17 * -----	1,2,4,5, 7-9	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 July 2001	Tyberghien, G

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 10 2249

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

09-07-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1032120 A	30-08-2000	NONE	
EP 0837559 A	22-04-1998	JP 10126164 A	15-05-1998
		JP 10190379 A	21-07-1998
		CN 1183673 A	03-06-1998
		US 5973557 A	26-10-1999